PHOTOMASK

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Comparison of Lithographic Performance between MoSi Binary mask and MoSi Attenuated PSM.

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ABSTRACT

The mask error budget continues to shrink with shrinking DRAM half pitch and MPU gate size year by year. The ITRS roadmap calls for mask CDU to be cut in half by 2014.[1] Both mask maker and mask user must take advantage of various mask properties, OPC strategies and resolution enhancement techniques to drive improvements. Mask material selection impacts both lithographic performance and mask manufacturability. In turn mask material properties and manufacturing techniques impact our ability to meet the technology roadmap. Studies have shown the advantages of polarized light[2,3] as well as the impact of various mask materials on high NA lithography.[4] In this paper we select the recently introduced binary mask material made from a MoSi absorber called Opaque MoSi On Glass (OMOG) for comparison with the conventional 6% att. PSM and 20% att. MoSi PSM. Through simulation and wafer prints, we optimized mask feature from viewpoint of MEEF and maximum exposure latitude (EL). The MoSi att. PSMs suffer from higher MEEF, which is attributed to the negative effect of TE polarization for mask duty cycle of 50% for 50 nm half pitch and below. Therefore a lower mask duty cycle is required for att. PSM to bring the MEEF performance back to acceptable levels. Experimental results confirm simulation results. As a result of the

Continues on page 3.

Table 1. Exposure method and optical conditions.

hp(nm)	60	50	45	40	38	38	32	22
Exposure Method	Single Exposure						Double Patterning	
Actual hp(nm)	60	50	45	40	38	38	64	44
NA	1.2	1.35					1.1	1.35
Illumination	Annular	cQuad				Dipole	Annular	cQuad
Outer	0.85	0.85	0.85	0.98	0.98	0.98	0.85	0.98
Inner	0.65	0.65	0.65	0.81	0.81	0.83	0.65	0.81
Blade Angle(°)		30	20	20	20	40		20

Table 2. Pitch ranges for through pitch evaluation.

Pitch Range (nm)	SRAFs	Selected Pitches (nm)
Minumum Pitch	No	90
Mid Range	No	100-150
Mid Range	Yes	180-190
200's	Yes	240-270
400's	Yes	400-480

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For new developments in technology
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For a list of meetings
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SPIE

EDITORIAL

Waiting for a chinook

Bob Naber, Principal at enableDFM

If you have attended a locally known offshore "immersion workshop", you might think this will be about salmon fishing and when will it ever return. If we have enjoyed a meal together you might think this could be a restaurant review. Good guesses but I was reminded of a famous American painting "Waiting for a Chinook" by Charles M. Russell while recently attending Semicon West and the Design Automation Conference. The painting depicts the remaining steer of a herd of 5000 during the most extreme winter of 1886 surrounded by hungry coyotes. A Chinook is also the warming wind caused by adiabatic heating of air flowing down the leeward side of a mountain so desperately desired during these extreme conditions. While our industry is experiencing the worst down turn in history from a combination of cyclicality combined with various financial and confidence effects, there was also cautious optimism that the worst was behind us and perhaps our industry's "Chinook" was beginning as I attended presentations and met with various attendees and exhibitors.

Dan Tracy, senior director of industry research and statistics for SEMI, reported on encouraging signs in data gathered from SEMI's members. "Our consensus is that the third quarter will be a good quarter. We have hit bottom, something that clearly played out in the last couple of months" in his market outlook presentation.

Following Semicon was the Design Automation conference which was decidedly more upbeat continuing the anticipation that a "Chinook" could be occurring.

Most recently we have the news:

1: That foundry utilization rates have improved from a low of 35% in Q1 to 68% in Q2 with Q3 predicted to be 78% by Gartner's Dean Freeman at a recent SEMI forum lunch.

2: SEMI reports that capital equipment book to bill is 1.06 which is above 1 for the first time since Jan 2007!

3: intel "ups" Q3 guidance 500M$ based on stronger than expected demand

You are probably most interested in the photomask segment and fortunately the premier event to get the latest information is upon us with SPIE / BACUS 29th Photomask Symposium Sept 14-17 in Monterey Chaired by Larry S. Zurbrick, of Agilent Technologies, Inc. and Warren Montgomery, College of NanoScale Science and Engineering (CNSE) and SEMATECH Inc. Details at www.spie.org

The keynote "Global Collaboration in Semiconductors and Strategies for the Mask Industry" will be by SEMATECH CEO Dr. Michael R. Polcari.

The symposium closes with a Special Session moderated By Warren Montgomery, Symposium Cochairman and Wolf Staud, Applied Materials on "Technology and Cost Issues Associated with Advanced Mask Making Solutions: Are Photomasks a Commodity?"

Join us in Monterey, I predict a warming trend!

BACUS

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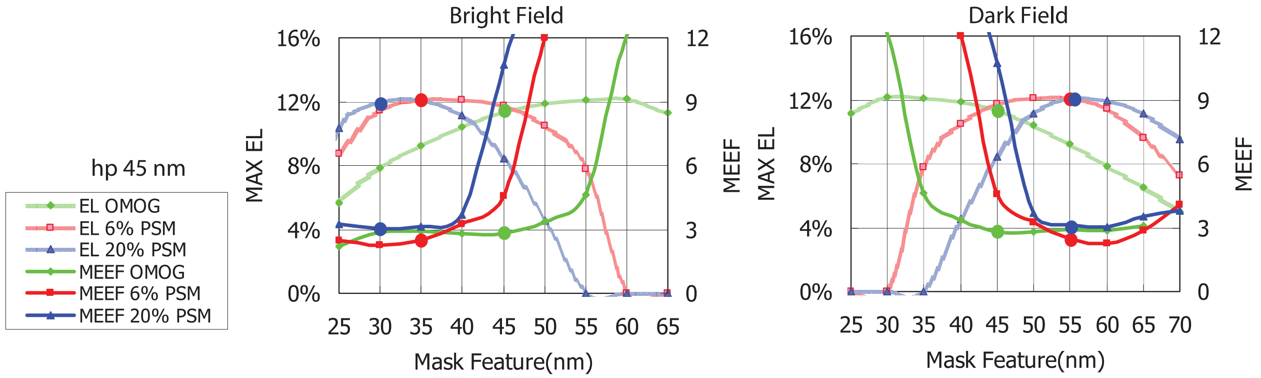

Figure 1. Maximum exposure latitude and MEEF as a function of mask feature size: dots represent optimized mask feature.

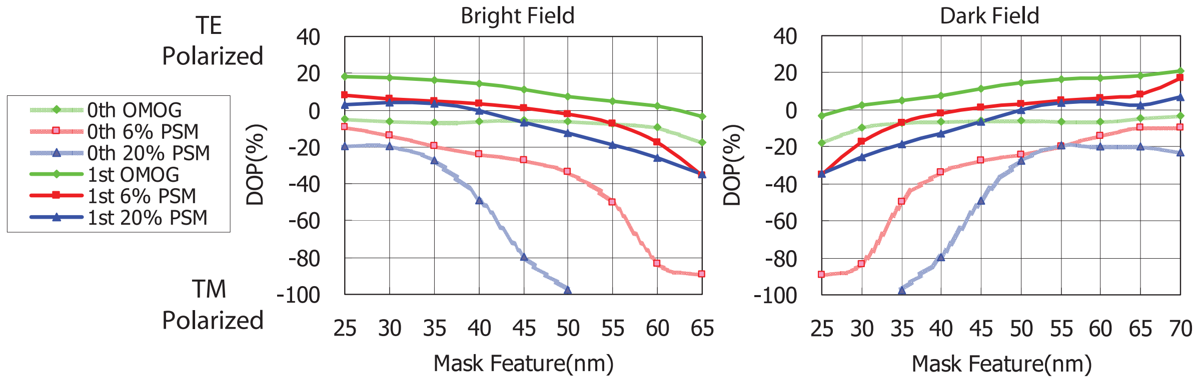

Figure 2. DOP through mask feature.

lower mask duty cycle, the att. MoSi PSMs exhibit poor Sub Resolution Assist Feature (SRAF) printability. On the contrary, the MoSi binary mask delivers both acceptable MEEF and acceptable SRAF printing performance. Moreover, we found that the mask structure impact of OMOG to wafer CD is smallest among three masks. OMOG gives the best combination of lithographic performance and delivery compared to the MoSi att. PSMs.

1. Introduction

Since the introduction of 193nm lithography, the 6% att. PSM mask has been the standard material for critical layers. Now with the development phase for 32nm and 22nm nodes well underway, we see that lithography conditions are much different from the initial introduction of 193nm lithography. The increase in NA, the adoption of immersion lithography and the use of polarized light make it interesting and meaningful to compare lithographic performance between binary and att. PSM masks.

MoSi binary mask called Opaque MoSi On Glass (OMOG) has been developed.[5] A thin Cr is used as a hard mask to minimize loading effects.[5] The thin hard mask enables us to reduce resist thickness. This in turn improves resolution capability. Moreover it was reported that exposure latitude (EL) and MEEF of OMOG was better than Cr binary mask.[5] Then OMOG was focused as a binary mask. In addition to the OMOG (binary) and 6% att. PSM, we also evaluated a 20% att. PSM to investigate the impact of att. PSM transmission on lithographic performance.

Table 3. Optimized mask feature size (nm).

	OMOG	6% PSM	20% PSM
Bright Field	45	35	30
Dark Field	45	55	55

Lithographic performance of OMOG, 6% att. PSM and 20% att. PSM in both bright field and dark field was simulated. Firstly we optimized mask feature at minimum pitch from viewpoint of maximum EL and Mask Error Enhancement Factor (MEEF). The resulting optimized mask features were different among three masks. We believe that the observed differences in optimal mask bias between materials are attributed to the differences in the degree of polarization induced by each material.

Generally, Sub Resolution Assist Feature (SRAF) use is an indispensable technique to provide adequate depth of focus (DOF) for larger pitches on layers with lithography settings that are optimized for denser pitches. But SRAF width will Photomask and Next-Generation Lithography Mask Technology XVI, edited by Kunihiro Hosono be critical issue with shrinking design rule. Next we investigated the impact of the optimized mask feature size on through pitch performance that includes the use of SRAF. SRAF printability between materials and across various pitches through simulation and experimental wafer results were compared. Wafer CD error was estimated to decide which mask was best. Finally, mask cycle time to further differentiate the mask materials were compared.

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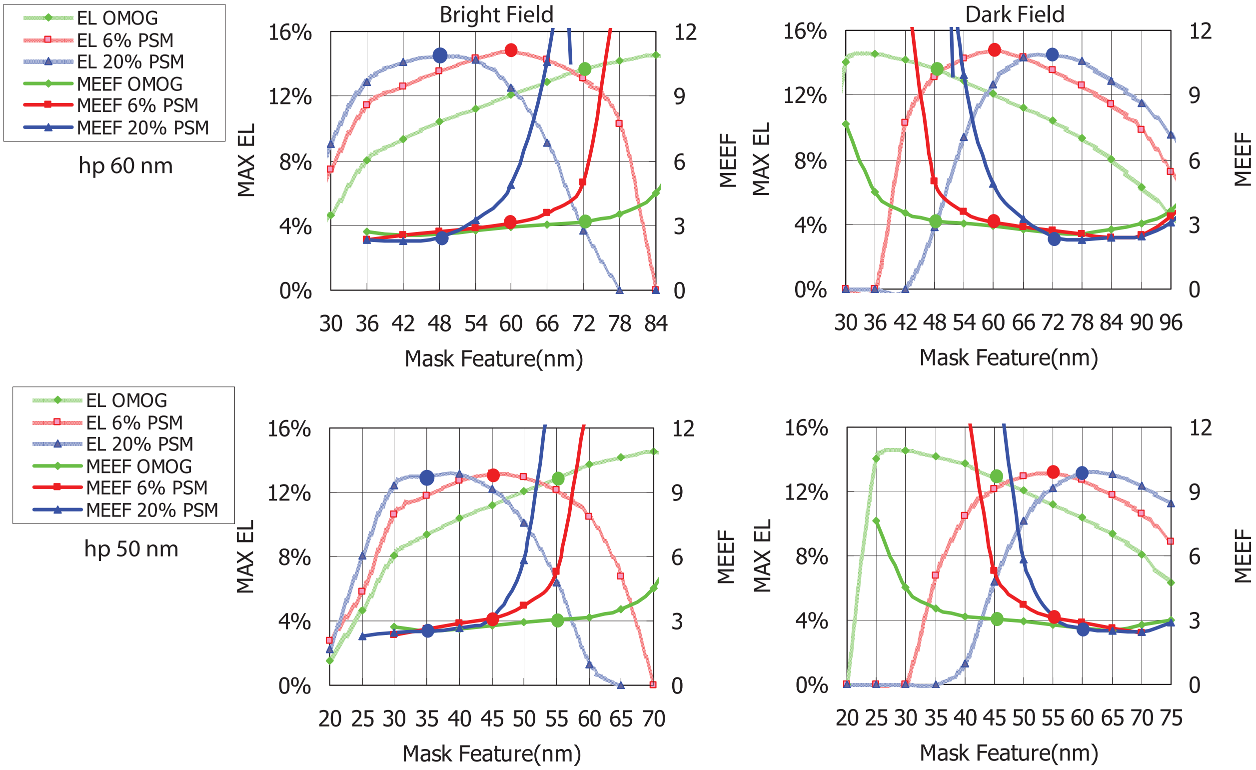

2. Simulation and experimental condition

Lithographic performance of line and space such as MEEF, maximum EL and depth of focus (DOF) was calculated with rigorous simulation. Prolith version 11 (KLA Tencor) using Maxwell Simulation Mode and a 3D mask structure was selected for all simulations. Structures from half pitch (hp) 60 nm to hp 22 nm were simulated. Table 1 summarizes the lithographic condition of each hp.

NA was increasing with shrinking hp. An annular illumination type was selected for hp 60nm. However, cQuad illumination was selected for 50nm hp and below to obtain higher resolution capability. As for hp 38nm, dipole illumination setting was also used because hp 38nm was considered to be severe for single exposure. CD target on wafer was basically equal to hp. Generally resolution limitation was defined in Equation (1)[6];

$$\text{Resolution Limit} = \lambda/4NA = \text{hp } 35.7 \text{ nm} \qquad (1)$$

Based on Eq. 1, the resolution limit is 35.7nm hp when λ is 193nm and NA is 1.35. Therefore double pattering is required to achieve hp 32nm and hp 22nm. The final target pitch is doubled for each lithography step in double patterning. Thus, the actual half pitch is two times larger than each hp. Wafer target CD was also optimized. Final target wafer CD could be achieved through etch slimming in bright field and certain shrinking techniques in dark field.[7,8] MEEF, EL, and DOF were simulated. EL and DOF were calculated based on ±10% CD variations.

SRAF width for isolated patterns was evaluated. Isolated pattern was defined as follows;

$$\text{Isolated pitch} = (\text{ Anchor pattern pitch} + 10 \text{ nm }) \ \lambda\ 5 \qquad (2)$$

Anchor pattern is the dense line and space pattern for each hp. Two SRAFs were placed beside main pattern. The pitch between main pattern and SRAF and the pitch between the two SRAFs was the anchor pattern pitch plus 10nm. Target wafer CD was hp plus 10nm in dark filed. This takes into consideration the CD shift between resist CD and etch CD. The large as possible SRAF that show good printing performance was chosen. SRAF printability was evaluated over a CD±15% process window. The DOF of the isolated pattern was compared for each material. Next we estimated CD error on wafer. We assumed ±1% as exposure dose variation and ±2 nm as mask global CD error and quartz depth variation. Finally, the impact of mask quartz depth variations on printed CD was also simulated. Experiments to confirm the simulation results were run using the ASML XT:1900i for both hp 45nm and hp 40nm conditions. Optical conditions were matched with simulation settings. MEEF and maximum EL between experiment and simulation was compared. SRAF printability was also demonstrated experimentally. SRAF rule is shows in table 2.

3. Simulation relief

3.1 Maximum EL and MEEF of hp 45nm

At first we optimized mask feature from the viewpoint of maximum EL and MEEF. Figure 1 shows the maximum EL and MEEF as a function of mask feature (x1) for 45nm hp. For bright field features the flat part of the OMOG MEEF curve extends just beyond a 45nm mask feature or 50% duty cycle (DC). The OMOG maximum EL peak occurs beyond this point of the steeper part of the MEEF curve. Thus, we selected an optimized mask feature around 50% duty cycle for OMOG which occurs on the flat part of the MEEF curve. The flat part of the PSM MEEF curve occurs at a lower duty cycle. Here we choose 35nm mask feature for the 6% att. PSM and a 30nm

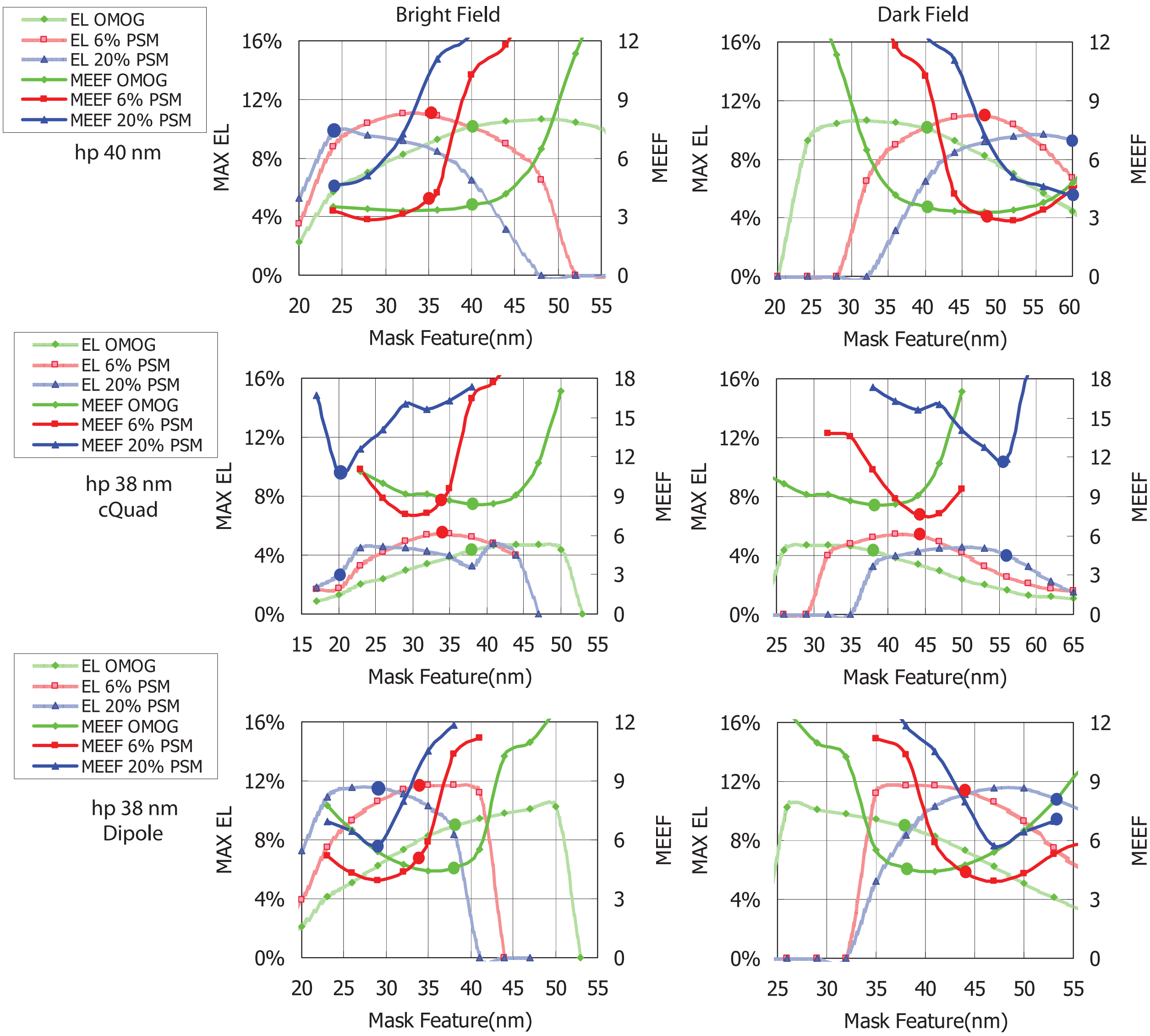

Figure 3. Maximum exposure latitude and MEEF as a function of mask feature size: dots represent optimized mask feature.

mask feature for the 20% att. PSM respectively.

The tendency of dark field is the reverse of bright field. Again we find that a 45nm mask feature is optimal for OMOG while a 55nm mask feature is optimal for the 6% and 20% PSM masks. Table 3 contains a summary of the optimized mask features used in our simulations.

3.2 Degree of polarization

Polarized illumination leads to an increase in contrast for hyper-NA immersion lithography.[3] All the components within the optical path, including the mask, must be compatible with this resolution enhancement technique. In order to explain the reason why the optimized mask features are different among three masks, the degree of polarization (DOP) was simulated. DOP is defined as follows:

$$DOP = (I_{TE} - I_{TM})/(I_{TE} + I_{TM}) \qquad (3)$$

Figure 2 shows DOP through mask feature for the OMOG and PSM masks. The more positive DOP the larger amount of TE polarized light. Conversely the more negative the DOP the larger amount of TM polarized light. TE polarized light is preferred over TM polarized light for imaging.[9] OMOG has less effect on degree of polarization through mask feature then either PSM masks. The PSM masks tend to result in TM polarized light (more negative DOP). For the PSM masks, the mask feature size where 0th order DOP starts to decrease rapidly corresponds to the rapid decline predicted for maximum EL and increase in MEEF shown in Figure 1. PSMs have the effect of stronger TM polarization at higher duty cycles. This is considered to be the reason for the deterioration in EL and MEEF for the PSM higher DC for bright field.

3.3 Expansion of EL and MEEF evaluation to various half pitch features.

Evaluation to different hp from 60nm to 22nm was expanded.

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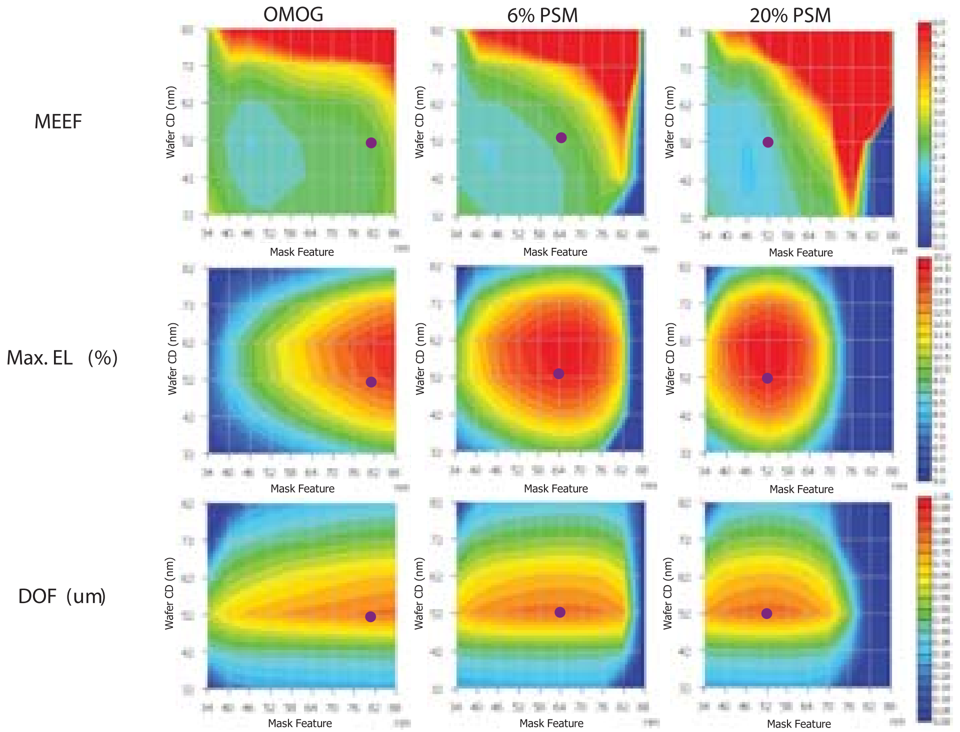

Figure 4. MEEF, max. EL and DOF through mask feature on hp 32nm in bright field: dots represent optimized mask feature.

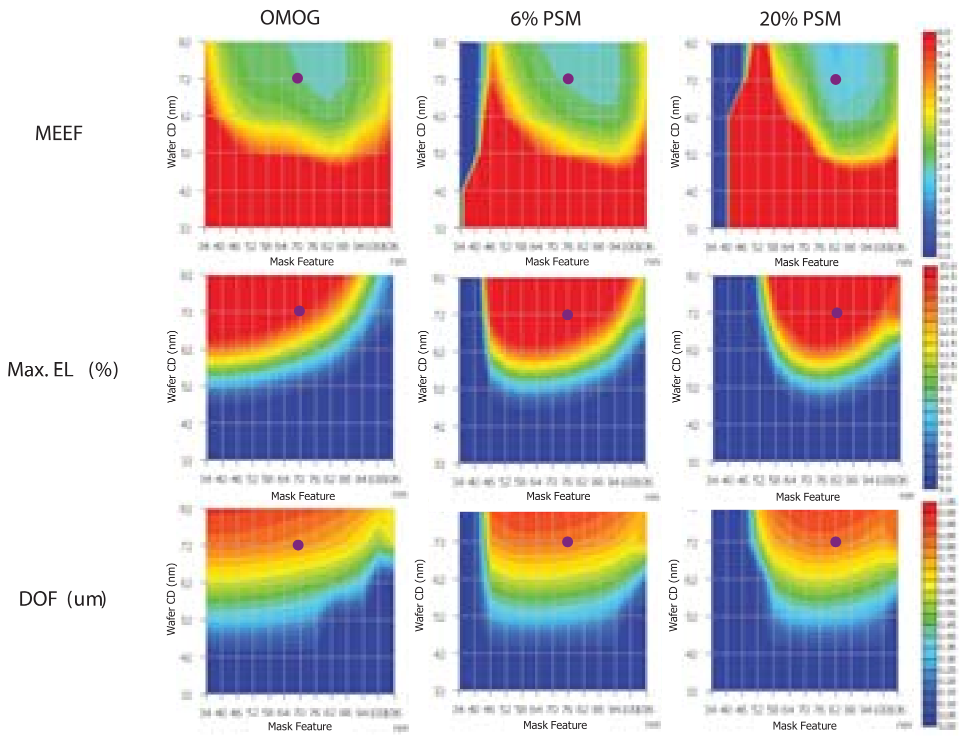

Figure 5. MEEF, max. EL and DOF through mask feature on hp 32nm in dark field: dots represent optimized mask feature.

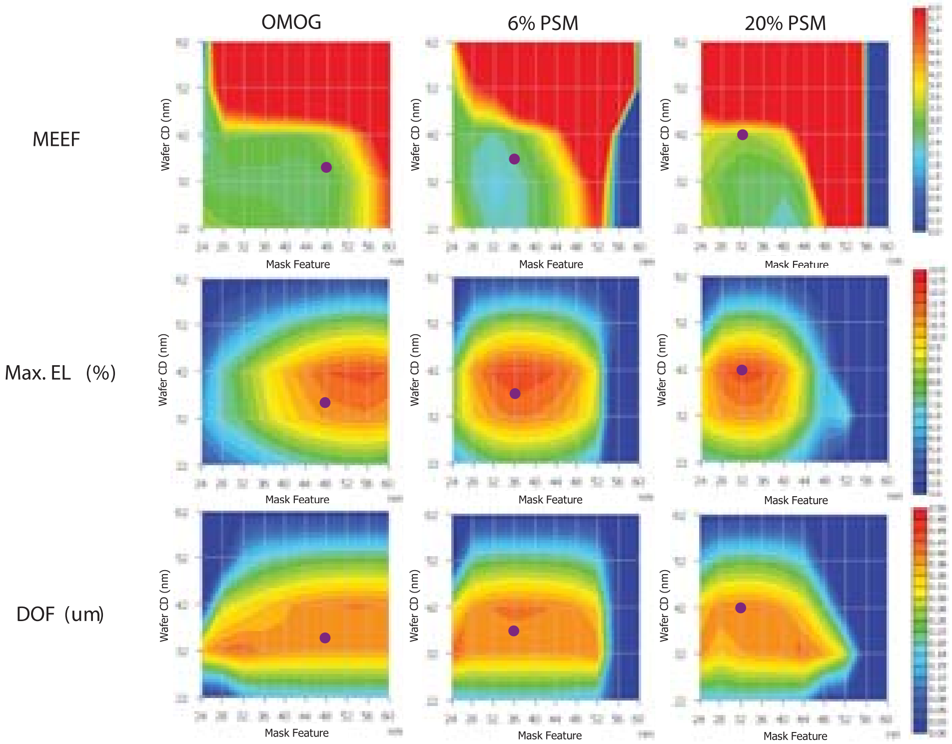

Figure 6. MEEF, max. EL and DOF through mask feature on hp 22nm in bright field: dots represent optimized mask feature.

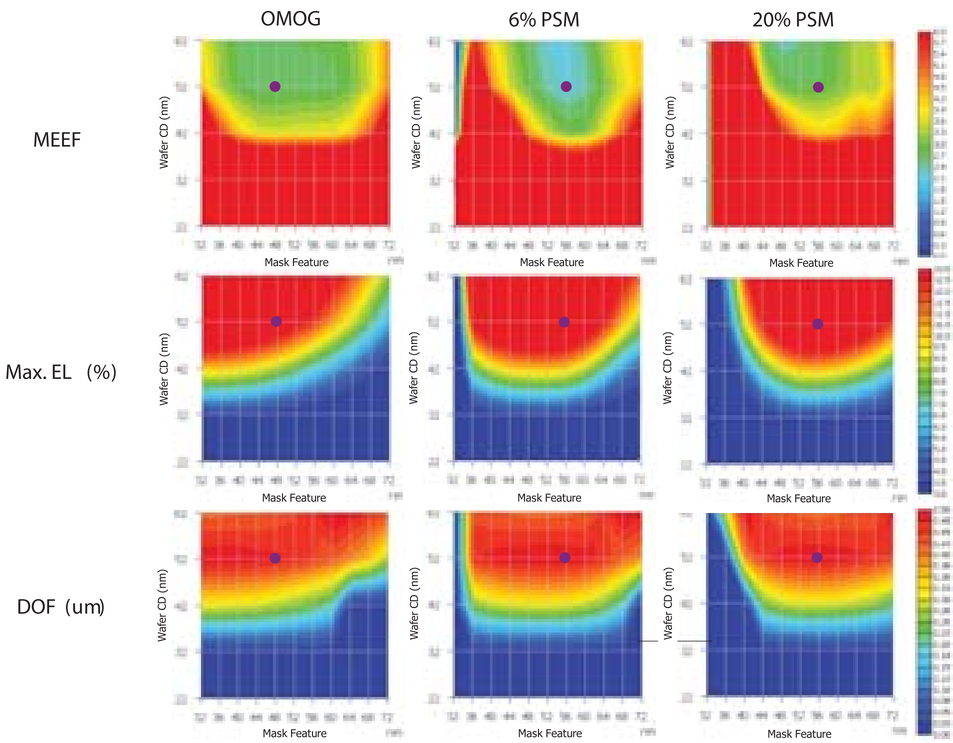

Figure 7. MEEF, max. EL and DOF as through mask feature on hp 22nm in dark field: dots represent optimized mask feature.

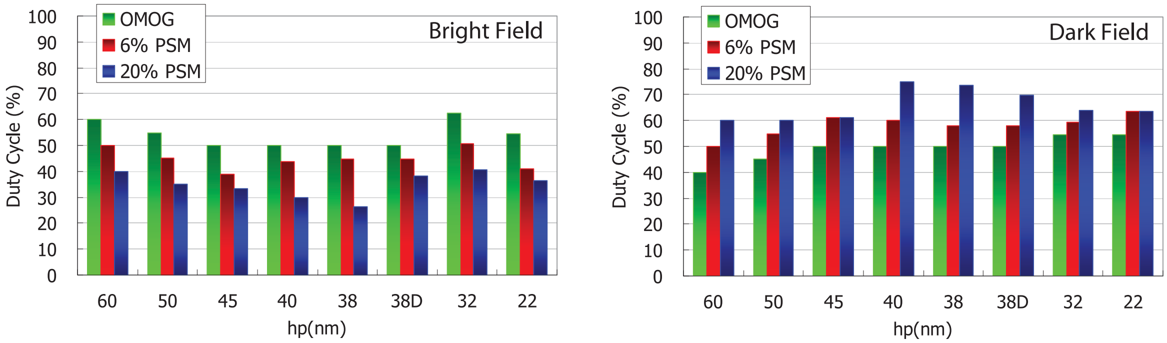

Figure 8. Duty Cycle: 38D represents hp 38nm with dipole illumination.

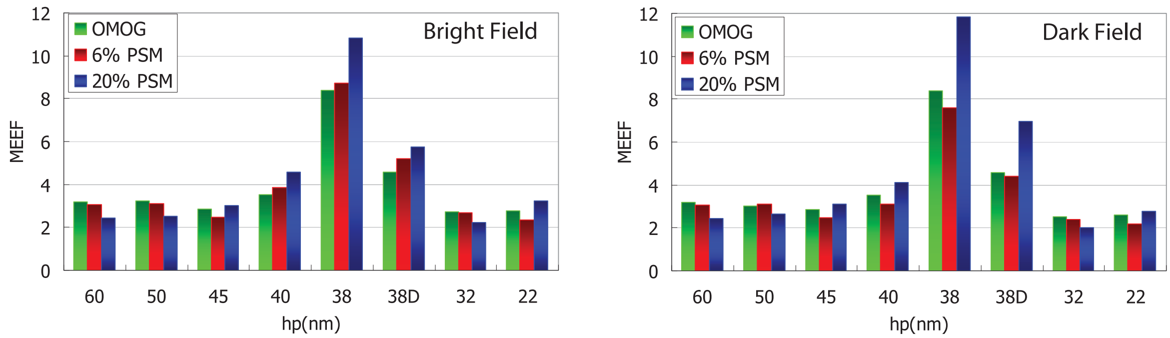

Figure 9. MEEF on various hp: 38D represents hp 38nm with dipole illumination.

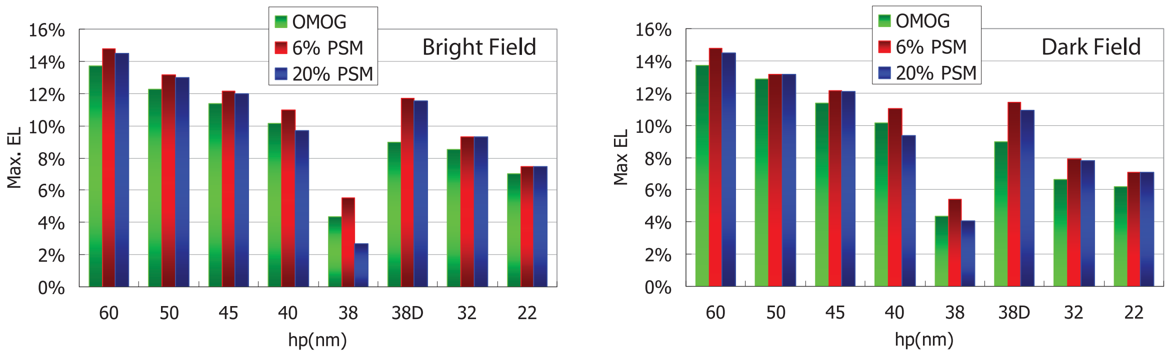

Figure 10. Maximum EL (CD±10%) on various hp: 38D represents hp 38nm with dipole illumination.

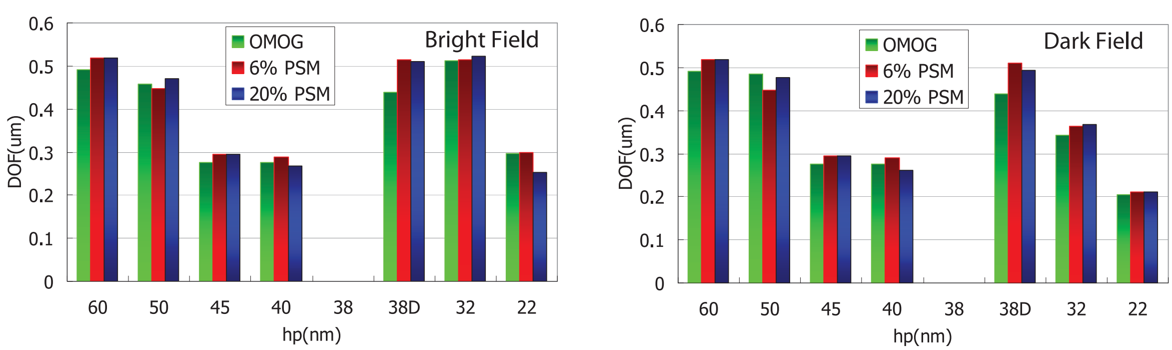

Figure 11. DOF of dense line of 5% exposure latitude on various hp: 38D represents hp 38nm with dipole illumination.

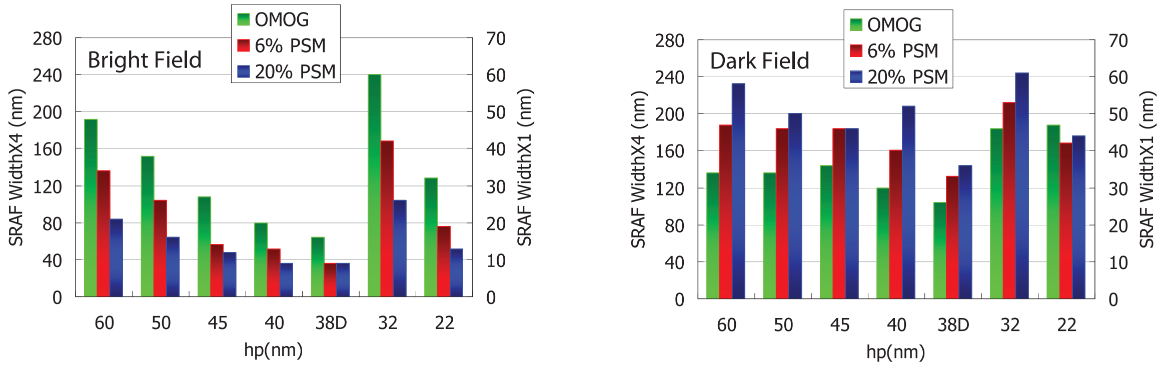

Figure 12. Optimized SRAF width on various hp: printability was evaluated within process window.

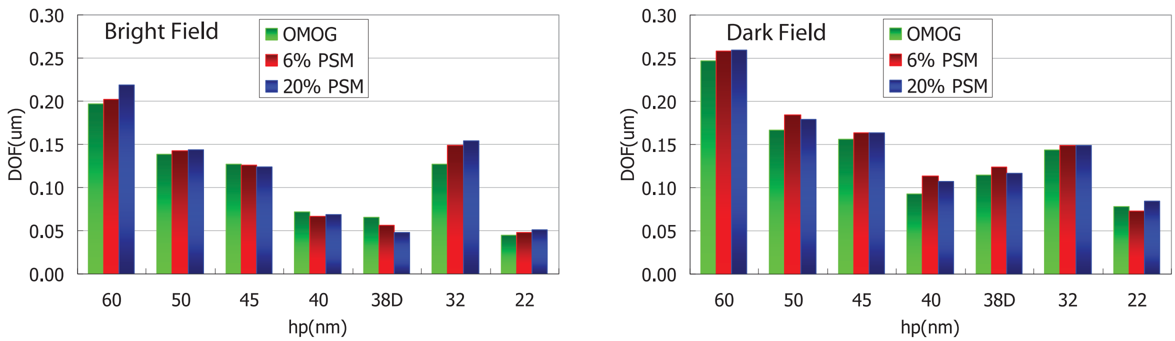

Figure 13. DOF of isolated pattern with SRAF under the condition of EL 5%.

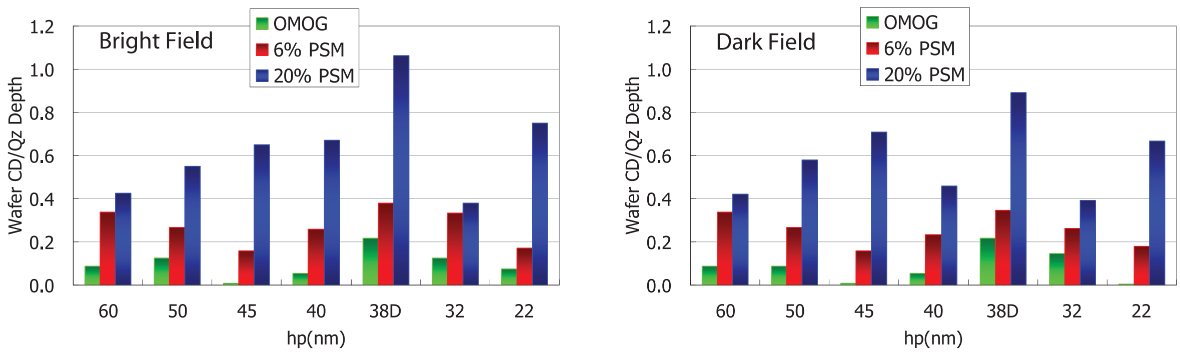

Figure 14. Quartz depth variation impact on wafer CD.

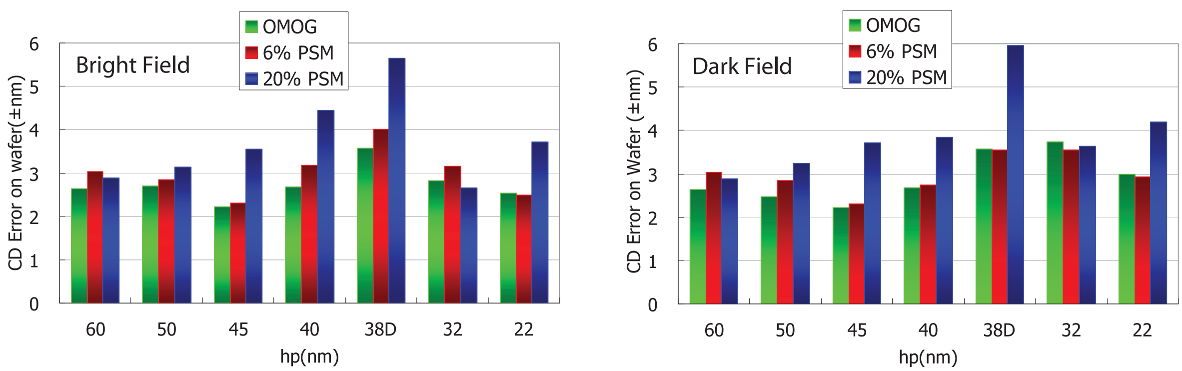

Figure 15. CD Error on wafer estimated from MEEF, quartz depth variation, and exposure dose variation.

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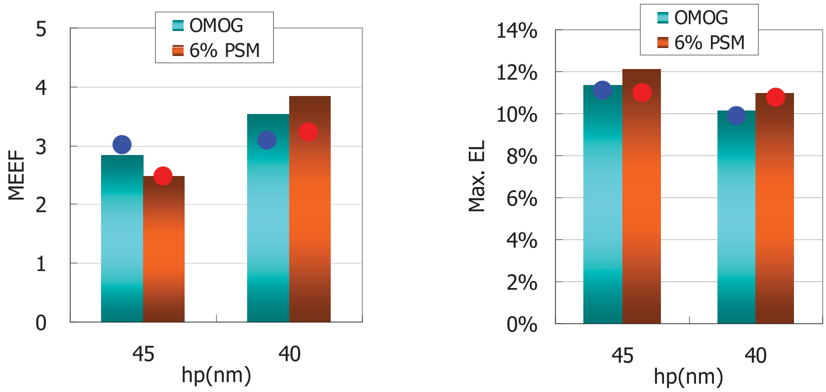

Figure 16 MEEF and maximum EL: dots represent experimental results and bars represent simulation.

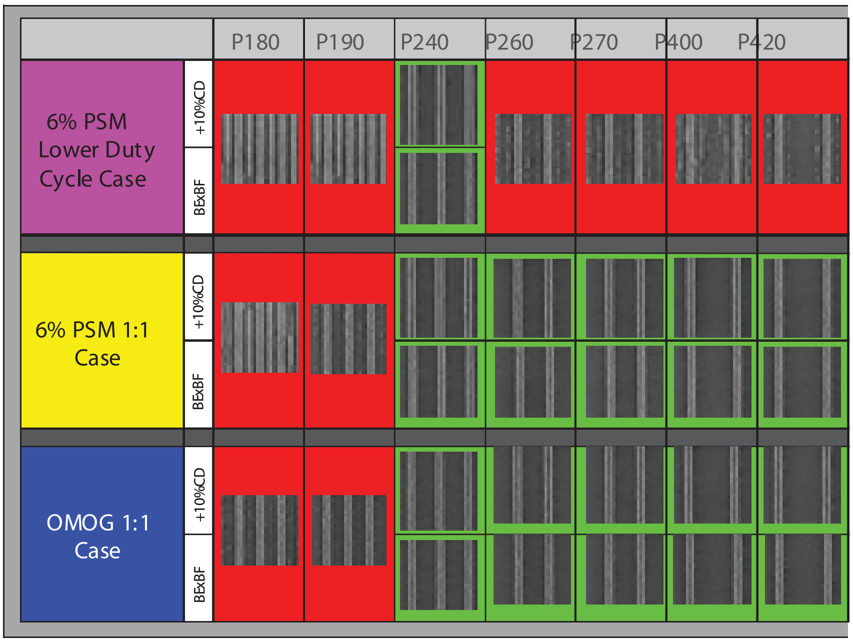

Figure 17 Experimental results of SRAF printability through pitch: red color represents that SRAF is printed, green color represents that SRAF is not printed through process window.

Figure 3 shows maximum EL and MEEF through mask feature for various hp. The illumination conditions for the various half pitches are shown in Table 1.

For bright field features the optimized mask feature for OMOG shifts to higher duty cycles for the 60nm hp as shown in Figure 3. We observed similar shift away from 50% DC but in the opposite direction for the dark field features. We also see for the hp 60nm that the optimal mask feature for the 6% & 20% att. PSM shift towards lower duty cycles for bright field and higher duty cycle for dark field. The same tendency was seen for hp 50nm. As for 40nm hp and below, the optimal mask feature for OMOG is around 50% duty cycle. The optimal mask feature for 6% and 20% PSM continue to shift to small duty cycles for bright field and larger duty cycles for dark field. This trend is observed for both cQuad and dipole illumination.

An ultimate resolution limitation is considered to be hp 35.7nm for NA1.35. We simulated lithographic performance of hp 32nm and 22nm with double patterning technique. The actual hp is 2 times larger than the final hp. But it seems to be difficult that we make CD target on wafer hp. Typically a wafer CD shrink technique such as etch slimming in bright field and shrinking in dark field can be used to adjust litho CD targets to final CD targets. We attempt to optimize both wafer CD and mask feature simultaneously. Figure 4 shows the dependence of MEEF, maximum EL and DOF on wafer CD and mask feature for the 32nm hp bright field case. The horizontal axis shows mask feature while the vertical axis shows the wafer CD. The actual pitch is 128nm. The optimum wafer CD for all masks is around 52nm because the DOF is at a maximum. The optimal mask feature was selected based on MEEF and maximum EL. Figure 5 shows dark field case. Here a 72nm wafer CD was selected for the dark field case. The optimized wafer CD in dark field is larger than that in bright field. Figure 6 shows hp 22nm bright field case. The actual pitch is 88nm. Here we see that the optimal wafer CD and mask CD are different for all three masks. For OMOG we choose a 34nm wafer CD with a 48nm

mask feature. The optimum combination for 6% att. PSM is 36nm wafer CD and a 36nm mask feature. The 20% att. PSM requires a 42 nm wafer CD with a 30nm mask feature. Figure 7 shows dark field case of hp 22nm. We decided 52nm wafer CD is optimized value. We also optimized mask feature from viewpoint of MEEF and maximum EL.

3.4 Lithographic performance

Figure 8 shows duty cycle of each hp for bright field and dark field. The order of higher DC for bright field features was OMOG, 6% att. PSM and 20% att. PSM. On the contrary, the order in dark field was 20% att. PSM, 6% att. PSM and OMOG. DC of OMOG was around 50% except hp 60nm in both bright field and dark field and hp 32nm in bright field.

MEEF is shown in Figure 9. MEEF of hp 38nm with cQuad illumination is very large. Even with dipole illumination, the MEEF is larger than other hp. The MEEF for the 20% att. PSM shows higher MEEF for hp 40nm and below when it is compared to the other materials. The MEEF for OMOG is comparable with 6% att. PSM across the entire range. Figure 10 shows maximum EL. Maximum EL shrinks with decreasing hp. The maximum EL for PSMs is slightly larger than for OMOG. The DOF, shown in Figure 11, is calculated based on 5% EL. The DOF differences are very small between the three masks. On the other hand, there is big difference between hp 50nm and hp 45nm due to the same NA used for both cases. We could not obtain hp 38 nm DOF with cQuad illumination. It can be said that cQuad is not practical use on hp 38nm. Contrarily, wide DOF was obtained with dipole illumination.

3.5 Sub Resolution Assist Feature (SRAF) width

Figure 12 shows the optimized SRAF width (4x) for an isolated pattern. In bright field, the SRAF width for OMOG is comparatively large. In spite of hp 38nm, SRAF width is larger than 60nm (15nm:1x). However, SRAF width of PSMs is less than 40nm (10nm:1x) on hp 40nm and 38nm. The small SRAF widths impact mask manufacturability. Both CD accuracy and pattern collapse during processing are concerned. It can be said that large SRAF width is benefit of OMOG. Although the required SRAF width for dark field structures is smaller for OMOG then PSM, the assist feature slots are slightly larger and are not as impacted by pattern collapse. The reason is considered that MEEF of isolated pattern with SRAF in bright field is larger than that in dark field. Large MEEF induces comparatively large SRAF width. The minimum SRAF width of OMOG in dark field is about 100nm (25nm:1x). SRAF widths in the range of 100nm (25nm:1x) are well within the current mask manufacturing capability. The DOF for an isolated pattern with SRAF is shown in Figure 13. The difference among masks is very small. If we assume DOF specs are 0.1um, DOF of hp 40nm, 38nm and 22nm is out of specs. In order to obtain enough DOF, we must optimize illumination from viewpoint of both dense pattern and isolated pattern.

3.6 Quartz depth variation impact

Figure 14 shows the slope of wafer CD to quartz depth. The impact to wafer CD of quartz depth variation on OMOG is very small since there is no phase restriction. However, there is a significant impact of quartz depth variation observed for PSM. This is especially true for a 20% att. PSM. Small slope of OMOG is advantageous from viewpoint of CD control on wafer.

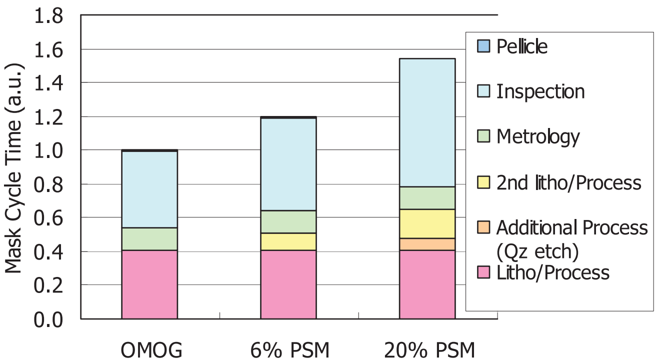

Figure 18. Manufacturing TAT: mask materials OMOG, 6% att. PSM, 20% att. PSM.

3.7 CD error on wafer

We estimated CD error on wafer caused by global mask CD error, quartz depth variation and exposure dose variation from simulation results. We assumed glolbal mask CD error is ±2nm, quartz depth variation is ±2nm and exposure dose variation is ±1%. CD error on wafer is shown in Figure 15. As a result, the difference of CD error among three masks increases with decreasing hp. The CD error observed for the 20% att. PSM is very large for 45nm hp and below. This is primarily driven by the wafer CD sensitivity to quartz depth variation. CD error of OMOG is slightly smaller than 6% att. PSM. Small wafer CD error on wafer is one of benefits of OMOG.

4. Experimental results

Figure 16 shows MEEF and maximum EL experimental results for OMOG material for bright field features. The difference between experimental results and simulation is relatively small. Thus, we believe that our simulation accracy is high.

We also evaluated SRAF printability for hp 45nm through pitch on wafer. Earlier we optimized the duty cycle for the hp 45nm for each material. Based on the required dose to size 45nm on wafer, we expanded our evaluation through pitch to included pitch ranges where SRAFs are required to maintain acceptable depth of focus. Figure 17 shows the wafer results for the lower duty cycle (39% DC) 6% att. PSM case, the 1:1 (50% DC) OMOG case and the 1:1 (50% DC) 6% att. PSM case. The SRAF size and mask bias was configured to target 45nm on wafer with the required dose to size. The minimum SRAF used was around 80nm at 4X.

Ealier we showed that both the 6% and 20% att. PSM show improved MEEF performance at lower duty cycles for hp 45nm bright field structures. However, when we try to expand the optimized setting through pitch for the 6% att. PSM we find that these settings result in poor SRAF printability. We also show that shifting to a higher duty cycle (50% DC) for hp 45nm improves printing performance for the 6% att PSM. However, under these conditions, we expect a higher MEEF at the minimum pitch for hp 45nm due to the negative effects from polarization. There is trade off between MEEF and SRAF printability for the att PSM. On the contrary, the OMOG gives the best combination of SRAF printability and lower MEEF.

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5. Mask cycle time

Mask cycle time continues to be a critical factor for many mask users. We estimated mask cycle time for each material in Figure 18. The cycle time for the two PSMs is comparatively larger. Especially, the cycle time of 20% att. PSM is true because of additional quartz etching. The OMOG enjoys a smaller cycle time due the shorter process procedures. Specifically a second write is required for the PSM but not for the OMOG. Moreover, OMOG benefits from reduced inspection frequency. Overall, the OMOG mask cycle time is almost 20% faster compared to the 6% att. PSM.

6. Conclusion

We compared lithographic performance such as MEEF, EL, DOF and SRAF printability between OMOG, 6% att. PSM and 20% att. PSM. We showed that the various materials can deliver similar lithographic performance for both bright and dark field structures for hp 45 nm and below if the mask duty cycle is optimized. However, only the OMOG delivers good lithographic performance at the densest pitches and acceptable SRAF printing at the larger pitches. An evaluation of factors that impact CD uniformity shows that the att. PSM masks are more susceptible to variations in quartz etch depth control. Finally the OMOG enjoys a 20% shorter mask cycle time due to the reduced processing content. We concluded OMOG is promising as a mask for both single exposure and double patterning in bright field and dark field.

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Industry Briefs

Sematech Seeks EUV Mask Tool Funding

By **David Lammers,** Semiconductor International

Few commercial suppliers are stepping up to develop the EUV mask inspection tools that will be needed for 22 nm EUV patterning, said Bryan Rice, director of lithography at Sematech. The consortium organized a meeting at SEMICON West of government, consortia and private industry leaders to develop financial support for the EUV mask infrastructure.

With few tools in development for the EUV mask infrastructure, Sematech convened a meeting during SEMICON West to garner financial support from companies and government sources. The goal is to entice commercial suppliers to develop EUV mask blank inspection, mask defect review, and mask pattern inspection tools.

"We are approaching all companies, consortia and government funding agencies, in a broad-based effort to obtain funding from all sources," said Bryan Rice, director of lithography at Sematech. Some optical inspection tools, such as the M7360 mask blank inspection tool from Lasertec, have been adapted to EUV inspection and might serve the needs of the pilot lines using EUV lithography. However, Rice said the Lasertec tool, and the KLA-Tencor mask pattern inspection tools, are targeted at 32 nm half-pitch (HP) designs. In particular, the high- volume manufacturing (HVM) solutions needed for 22 nm manufacturing "do not exist, and funding is a big problem," he said.

Sematech's goal is bring EUV scanners into corporate pilot lines by 2011 to support 22 nm HP development. By 2013, plans call for EUV to be in use for HVM lines. Although EUV source development remains a major challenge, Rice said companies are funding source and resist development, providing hope that solutions will arrive in time. The mask infrastructure, however, is a different story.

"Mask blank inspection tooling has no commercial suppliers who have committed to building the tool," Rice said, with identical challenges in mask defect review and mask pattern inspection. Sematech has decided to fund a yet-to-be-identified supplier for the mask deposition tool. The strategy is to find a bridge tool supplier for an aerial imaging measurement system (AIMS) tool that initially would have the capability to support the pilot lines expected in the 2011 time frame, he said.

To date, Rice said, nearly all the funding in support of the mask infrastructure has come from Sematech. The consortium will devote most of its lithography budget over the next four years to the mask infrastructure issue, as it tries "to find funds and identify suppliers. To that end, we have a workshop planned in conjunction with SEMICON West to get the leaders of the EUV community to tackle this specific problem."

Self-Aligned Double-Patterning Litho Gains Steam

By **Mark LaPedus,** EE Times

For next-generation memory production, 193-nm lithography with self- technology of choices over rival schemes, according to an analyst.

"With the chip industry staying on Moore's Law and lithography stuck at the 193-nm wavelength, chip makers are looking to double patterning to drive linewidth shrinks," said C. J. Muse, an analyst with Barclays Capital, in a report.

In doubling patterning, an IC maker is essentially doubling the process steps and creating two masks, thereby boosting production costs. Double patterning can be implemented in three ways: litho-etch-litho-etch, litho-freeze-litho-etch, and the sidewall spacer approach, also called SADP.

"SADP is the technology of choice in NAND, with all players adopting SADP at the 32-nm node," Muse said. "In our view, SADP was really the only choice due to (i) inadequate overlay and line edge roughness capabilities of the then existing litho tools, (ii) the simple nature of NAND 1-D structure, and (iii) availability of excess etch and CVD tool capacity."

Going beyond 32-nm, SADP still has an edge. "Looking to the 22-nm node, our checks suggest that SADP is the preferred option for all the major NAND manufacturers as development is already underway and litho tools by themselves alone are not yet ready to satisfy the requirements at 22-nm," Muse said.

"At 22nm, it appears currently that SADP might be required for three layers—STI, gate and bit line—instead of only one layer at 32-nm," the analyst said. "And that would be expensive. This will likely prompt redesigns/workarounds of the NAND architecture and the process flow which might ultimately reduce the number of layers for which SADP needs to be adopted, at least at the manufacturers that are cash strapped. Another variable is that breakthroughs in EUV might insert EUV sooner than expected."

And what about DRAM? "But the story changes a bit for DRAM. DRAM offers a more complicated 2-D structure and has 3x as many critical layers at the 4x node and 9x at the 3x node—thus driving the cost of SADP that much higher," the analyst said. "This said, SADP is a proven technology and SADP is at least currently the "roadmap entry" for most DRAM makers for the 3x nm node."

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About the BACUS Group

Founded in 1980 by a group of chrome blank users wanting a single voice to interact with suppliers, BACUS has grown to become the largest and most widely known forum for the exchange of technical information of interest to photomask and reticle makers. BACUS joined SPIE in January of 1991 to expand the exchange of information with mask makers around the world.

The group sponsors an informative monthly meeting and newsletter, BACUS News. The BACUS annual Photomask Technology Symposium covers photomask technology, photomask processes, lithography, materials and resists, phase shift masks, inspection and repair, metrology, and quality and manufacturing management.

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Calendar

2009

SPIE Photomask Technology

14-17 September
Monterey Marriott and
Monterey Conference Center
Monterey, California, USA
spie.org/pm

SPIE Lithography Asia - Taiwan

18-19 November
Sheraton Taipei Hotel
Taipei, Taiwan
spie.org/la

Late abstracts will be considered by the Chairs

2010

SPIE Advanced Lithography

21-26 February
San Jose Marriott and
San Jose Convention Center
San Jose, California, USA
spie.org/al

Late abstracts will be considered by the Chairs

You are invited to submit events of interest for this calendar. Please send to lindad@spie.org; alternatively, email or fax to SPIE.

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